REMARKS

Claims 1-20 are pending in the application.

Claims 1-20 have been rejected.

Claims 1-20 remain pending in this application.

The Examiner is thanked for noting the informality of Claim 4. Claim 4 has been amended accordingly, and this objection is obviated.

Reconsideration of the claims is respectfully requested.

I. CLAIM REJECTION UNDER 35 U.S.C. §103

Claims 1-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,563,837 to Krishna, et al., hereinafter "Krishna". This rejection is respectfully traversed.

In ex parte examination of patent applications, the Patent Office bears the burden of establishing a prima facie case of obviousness. MPEP §2142, p. 2100-125 (8th ed., rev. 5, August 2006). Absent such a prima facie case, the applicant is under no obligation to produce evidence of nonobviousness. Id. To establish a prima facie case of obviousness, three basic criteria must be met: Id. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Id. Second, there must be a reasonable expectation of success. Id. Finally, the prior art reference (or references when combined) must teach or suggest all the claim

limitations. *Id.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *Id.*

Claim 1 of the present application currently requires:

For use in a fixed-size packet switch, a switch fabric comprising:

N input buffers to receive incoming fixed-size data packets from an input port at a first data rate and to output said fixed-size data packets at a second data rate equal to at least twice said first data rate, wherein said N input buffers are internal to said switch fabric and are external to said input port;

N output buffers to receive fixed-size data packets at said second data rate and to output-said fixed-size data packets to an output port at said first data rate, wherein said N output buffers are internal to said switch fabric and are external to said output port; and

a bufferless, non-blocking interconnecting network to receive from said N input buffers said fixed-size data packets at said second data rate and to transfer said fixed-size data packets to said N output buffers at said second data rate. (emphasis added).

Krishna fails to teach or disclose, for example, N input buffers that are internal to said switch fabric and are external to said input port. Krishna also fails to teach or disclose, for example, N output buffers that are internal to the switch fabric and are external to said output port, as currently required by Claim 1. In addition, Krishna fails to teach or disclose a bufferless, non-blocking interconnection network, as currently required by Claim 1.

At the very most, Krishna discloses combined input-output buffered network device that uses a non-blocking switch fabric, such as a cross-bar, operating at a speed-up of two. (Krishna, column 3, lines 60-67). Each input port 50, 51 and 52 contains input buffers "a" through "d" and each output port 59, 60 and 61 contains output buffers "a" through "d". (Id. at column 7, lines 5-14 and 49-53;

and Figures 1-17). The Krishna system teaches having cells that are placed into the next available input buffer "a", "b", "c" or "d" in the virtual output queue 56, 57 or 58 within the input port 50, 51 or 52. (Id. at column 7, lines 49-53; and Figures 1-17).

Krishna therefore fails to teach bufferless, non-blocking interconnection network where the N input buffers are external to the input port and the N output buffers are external to said output port, as required by Claim 1 and its dependents, Claims 2 and 3. Similar arguments are true for Claim 4 (and its dependents, Claims 5 and 6), Claim 7 (and its dependents, Claims 8-13) and Claim 14 (and its dependents Claims 15-20).

The Examiner's response appears to misread Krishna's teaching. The Examiner indicates that "channels 80-88 form crossbar 89, which does not include any buffers." This much, at least, is correct. Krishna teaches that "the network device of this invention uses a non-blocking switch fabric, such as a crossbar, operating at a speedup of two" (Col. 3, lines 63-65) and "Each input port 50, 51 and 52 is connected to each output port 59, 60 and 61 via connection channels 80 through 88, which form the switch fabric 89 of the network device 49. The switch fabric 89 is implemented as a crossbar in one embodiment" (Col. 5, lines 57-61).

Krishna is clear that connection channels 80-88 are the switch fabric 89, which is implemented as a crossbar. There are no buffers described with relation to connection channels 80-88 forming the switch fabric 89, or its implementation as a crossbar.

However, the claims require that the N input buffers are internal to the switch fabric. It is clear that Krishna's connection channels 80-88, forming the switch fabric 89 and implemented as a crossbar have no internal input buffers at all, and so cannot meet the clear limitation of the claims.

Similarly, the claims require that the N output buffers are internal to the switch fabric. It is clear that Krishna's connection channels 80-88, forming the switch fabric 89 and implemented as a crossbar have no internal input buffers at all, and so cannot meet the clear limitation of the claims.

The Examiner attempts to read the claimed limitations on Krishna's network device by ignoring Krishna's own clear description of its network device. By Krishna's own description, there are no input or output buffers internal to the switch fabric, as required by the claims. Krishna describes its input ports as connected to, and therefore separate from, the switch fabric.

Moreover, there is no suggestion or motivation within *Krishna* to prompt one of ordinary skill to selectively combine discrete elements from *Krishna* and then seek out still others as required by the claims of the present application.

Accordingly, Applicants respectfully request favorable reconsideration and the withdrawal of the §103 rejection.

NO. 1392 P. 15

OCT. 30. 2007 4:41PM

DOCKET NO. 01-HK-048 SERIAL NO. 10/036,809 PATENT

CONCLUSION

As a result of the foregoing, the Applicants assert that the remaining claims in the Application are in condition for allowance, and respectfully requests that this Application be passed to issue.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at wmunck@munckbutrus.com.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS CARTER, P.C.

Date: Uchher 30, 2007

William A. Munck Registration No. 39,308

P.O. Box 802432 Dallas, Texas 75380 (972) 628-3600 (main number) (972) 628-3616 (fax)

E-mail: wmunck@munckbutrus.com